Space Vector Modulation with DC-Link Voltage Balancing Control for Three-Level Inverters

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***Abstract*— Modified space vector modulation (SVM) for DC-link voltage balancing of three-level inverter is proposed here. Effect of the DC-link capacitor voltage deviation on inverter switching states is presented for three-level inverter. Pulse pattern arrangements for proposed SVM using degree of freedom available in choice of redundant space vectors, sequencing of vectors, and splitting of duty cycles of vector are best exploited. Seven-segment SVM scheme and modified closed loop space vector DC-link voltage balancing control schemes are implemented. The effectiveness of proposed scheme is verified by simulations and experimental verification on laboratory prototype.**

***Index Terms*— diode-clamped inverter, multilevel inverter, space-vector modulation, voltage source inverter**

I. INTRODUCTION

Multilevel inverters have gained much attention for the next generation medium voltage and high power applications. Three-level diode-clamped inverter also known as neutral point clamped (NPC) inverter is most favourable among various multilevel configurations explored in the literature. The three-level NPC inverter is used in this paper. Problems due to neutral-point voltage-unbalance and its various balance control methods are discussed at length [1]. DC-link unbalance may overstress the capacitors and devices during a sudden regenerative load increase, and it can also cause nuisance over voltage or under voltage trips. Active front-end converter with coordinated control from grid end and load end for DC-link balancing control is proposed [1].

The effect of capacitor voltage unbalance during transient and steady state condition are analyzed in this paper. In the worst case of unbalance one capacitor is fully charged to full DC-link voltage that results in double stress on the capacitor and the switching devices, reducing output waveforms to two-level from normal three-level. The effect of the zero sequence voltage on the neutral point variation and the dependence of DC-link voltage unbalance on the system parameters like load currents, load power factor, value of capacitance of capacitor, and modulation index have been extensively analyzed for three-level NPC inverter [2-3]. The neutral point balancing schemes, for the three-level neutral point clamped inverter, are based on the effective use of the redundant switching states of the inverter voltage vectors. The redundant switching states are used alternately such that the neutral point voltage unbalance caused by the first switching state is compensated by another state; thus, bringing the total unbalance in one switching cycle to zero [4-5]. Detailed study of NPC inverter, space vectors, dwell timings, and pulse pattern arrangement with division of middle regions for neutral point balance and even harmonic elimination scheme are addressed [5]. Neutral point voltage control is achieved by utilizing the phase current polarity and distribution of the redundant voltage vectors. A control strategy is proposed to maintain average current drawn from neutral-point to the minimum [6-7]. Hysteresis control for DC-link variation control and common mode voltage elimination in an open end winding induction motor fed from two three-level inverters from either side is investigated [8]. Mathematical modeling and neutral-point control with charge balance is proposed for four-level voltage source inverter [9]. ANN based neutral-point self-voltage balancing SVM with pulse pattern arrangement is discussed for NPC inverter. It requires extra switchings when reference vector changes sector. [10]. The problem of required extra switchings at sector changeover is eliminated in this paper. Mathematical modelling and Simulation results presented in [11] are experimentally validated on lab prototype in this paper.

The proposed SVM scheme effectively utilizes redundant switching states for the inverter voltage vectors which have unbalancing effect on the capacitor voltages. These switching states have opposite effects on the DC-link capacitor voltages. So, alternate use of these switching states are used for DC-link capacitor voltage balancing control. Effective utilization of redundant switching states eliminates the need of extra hardware for the capacitor voltage balancing, without affecting the dwell timing of space vector over switching period. The performance of various SVM schemes are evaluated with respect to inverter output voltage THD, current THD and neutral point voltage with respect to various DC-link voltages and modulation index (MI). The overall performance of proposed scheme appears to be attractive.

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II. THREE-LEVEL INVERTER

Figure 1 shows the simplified circuit diagram of a popular three-level neutral point clamped (NPC) inverter. The inverter leg 'a' is composed of four IGBT switches S_1 to S_4 with four antiparallel diodes D_1 to D_4. On the DC side of the inverter, the DC bus capacitor is split into two, providing a neutral point 'n'. When switches S_2 and S_3 are turned on, the inverter output terminal a is connected to the neutral point through one of the clamping diodes D_{n1} and D_{n2}. Ideally, the voltage across each of the DC capacitors is $V_{dc}/2$, which is half of the total DC-link voltage V_{dc}. With a finite value for C_1 and C_2, the capacitors can be charged or discharged by neutral current i_n, causing neutral-point voltage deviation.

As indicated earlier, the neutral-point voltage Vn varies with the operating condition of the NPC inverter. If the neutral-point voltage deviates too far, an uneven voltage distribution takes place, which may lead to premature failure of the switching devices and cause an increase in the harmonic of the inverter output voltage.

The operating status of the switches in the NPC inverter can be represented by the switching states shown in table I. Switching state 'P' denotes that the upper two switches in leg 'a' are on and the inverter pole voltage V_a, which is ideally $+V_{dc}/2$, whereas 'N' indicates that the lower two switches conduct, leading to $V_a = -V_{dc}/2$. Switching state 'O' signifies that the inner two switches S_2 and S_3 are on and V_a is clamped to zero through the clamping diodes. Depending on the direction of the load current i_a, one of the two claming diodes is turned on. For instance, a positive load current ($i_a > 0$) forces D_{n1} to turn on, and the terminal 'a' is connected to the neutral point 'n' through the conduction of D_{n1} and S_2. The switches S_1 and S_3 operate in a complementary manner similar to switches S_2 and S_4.

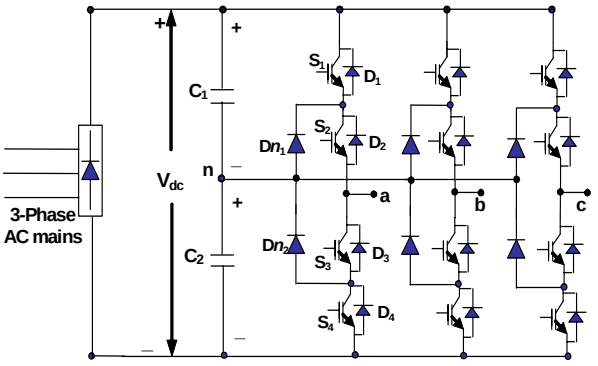

Figure 1. Three-level neutral-point clamped inverter topology

TABLE I
DEFINITION OF SWITCHING STATE

Switching State	Device Switching Status (Phase a)				Pole Voltage V_a
	S_1	S_2	S_3	S_4	
P	On	On	Off	Off	$+V_{dc}/2$
O	Off	On	On	Off	0
N	Off	Off	On	On	$-V_{dc}/2$

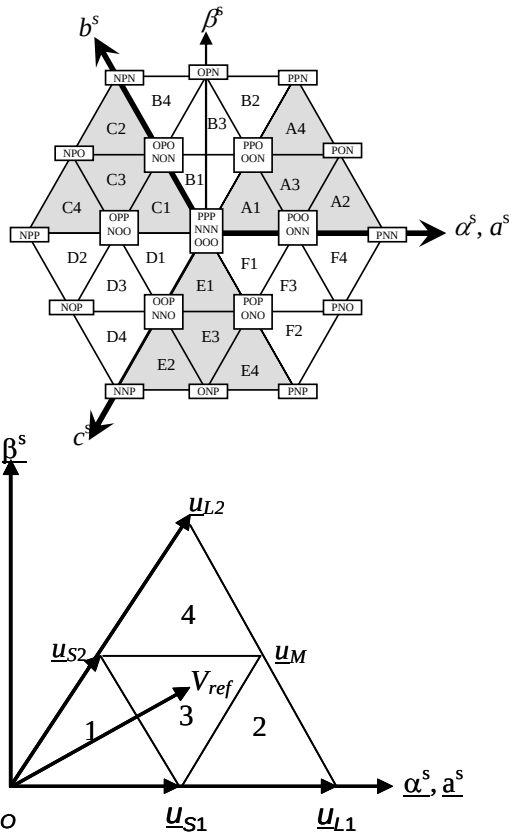

Figure 2. Space-vector diagram showing switching states (top) and Vector placement for SVPWM in sector A (bottom)

As indicated earlier, the operation of each inverter phase lag can be represented by three switching states P, O, and N. Taking all three phases in account, the inverter has a total of 27 possible combinations of switching states. Figure 2 shows space vector diagram of total 27 switching states corresponding to 19 voltage vectors for three-level NPC inverter. Figure 2 (bottom) shows vector placement in a sector A. Based on magnitude, the voltage vectors can be divided into four groups: Zero vector ($\mathbf{u_O}$), Small vector ($\mathbf{u_S}$), Medium vector ($\mathbf{u_M}$), and Large vectors ($\mathbf{u_L}$). All zero vectors have zero magnitude, small vectors have a magnitude of $V_{dc}/3$, medium vectors have magnitude of $V_{dc}/3$ and large vectors have magnitude of $2V_{dc}/3$. Each small vector has two switching states, one containing P and other containing N, and therefore can be further classified into a P-type or N-type vector.

III. EFFECT OF SWITCHING STATES ON NEUTRAL-POINT VOLTAGE DEVIATION

The effect of switching states on neutral voltage deviation is illustrated in figure 3. When the inverter is operated with switching state [PPP] of zero vector $\mathbf{u_O}$, the upper two switches in each of the three inverter legs are turned on, connecting the inverter terminals a, b, and c to the positive DC bus as shown in figure 3(a). Since the neutral point 'n' is left unconnected, this switching state

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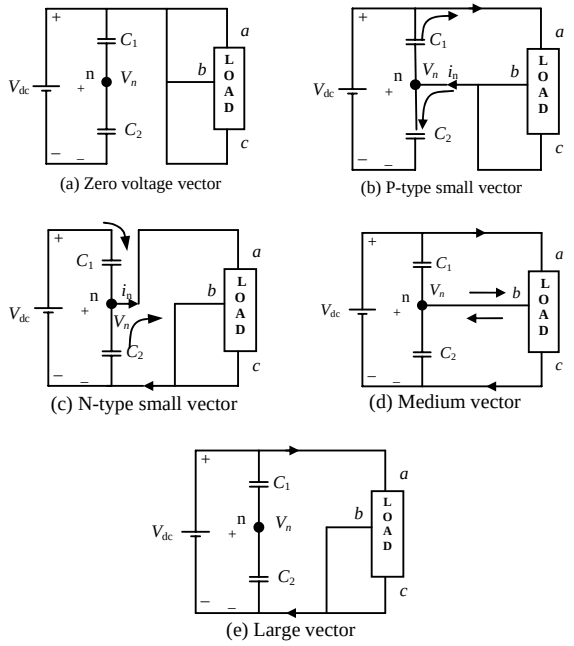

Figure 3. Effect of switching states on Neutral point voltage deviation

does not affect V_n. Similarly, the other zero switching states [OOO] and [NNN] do not cause V_n to shift either. Fig 3(b) shows the inverter operation with P-type switching state [POO] of small vector $\mathbf{u_{Sp}}$. Since the three-phase load is connected between the positive DC bus and neutral point 'n', the neutral current i_n flows in 'n', causing V_n to increase. On the contrary, the N-type switching state [ONN] of small vector $\mathbf{u_{Sn}}$ makes V_n to decrease as shown in figure 3(c). For medium vector u_M with switching state [PON] in figure 3(d), load terminals a, b, and c are connected to the positive bus, the neutral point, and the negative bus, respectively. Depending on the inverter operating conditions, the neutral-point voltage V_n may rise or drop. Considering a large vector u_L with switching state [PNN] as shown in figure 3(e), the load terminals are connected between the positive and negative DC buses. The neutral point 'n' is left unconnected and thus the neutral voltage is not affected.

IV. DC-LINK CAPACITOR VOLTAGE BALANCING SCHEME

Various space vector modulation (SVM) schemes have been proposed for the three-level NPC inverter using either open loop scheme or closed loop scheme [11]. This section proposes modified SVM scheme for better neutral point stabilization. To reduce neutral-point voltage deviation, the dwell time of a given small vector can be equally distributed between the P-type and N-type switching states over a sampling period. Either one small vector or two small vectors among the three selected vectors are available for nearest three vectors (NTV) selection according to the triangular regions in which the reference vector V_{ref} lies. When the reference vector V_{ref} is in region 2 or 4, only one small vector is in NTV where as in region 1 or 3 two small vectors are in NTV as shown in figure 2.

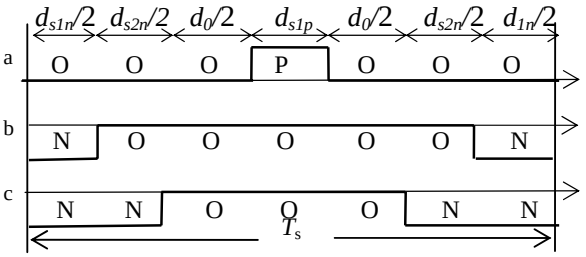

Figure 4. Pulse pattern arrangement for conventional seven-segment SVPWM in region A1

A. SVM-1 (7-Segment SVM)

SVM-1 is most widely used conventional 7-segment SVM. Seven-segment pulse pattern is chosen for all four regions in SVM-1. Its pulse pattern arrangement for region A1 is shown in figure 4. Seven segment SVM divides dwell time of only one small vector in P-type and N-type out of two small sectors available in region 1 and 3. Thus, neutral point deviation is not minimized in SVM-1.

B. SVM-2 (Close loop 7, 9 & 13-Segment SVM with delta correction in dwell time)

To reduce neutral-point voltage deviation according to the location of region, pulse pattern arrangement is optimized. Positive and negative sequences of modified SVM pulse pattern arrangement for regions A1, A2, A3, and A4 of sector A are shown in figure 5 for one sampling period. Here, two small vectors are used for neutral point voltage control for regions 1 and 3. As shown in figure 7 negative sequence (NEG_SEQ) pulse patterns are arranged in exact reverse order of positive sequence (POS_SEQ) pulse pattern and vice versa. Positive sequence and negative sequence are switched alternatively. Sequencing of various switching states in different sectors and regions for SVM-2 are shown in table II.

Numbers of switchings per phase in sampling period Ts for modified SVM are one in region 2 or 4, two in region 1 and one or two in region 3. In conventional SVM as shown in figure 6 two switching per phase are required in sampling period T_s. Here, T_s is sum of dwell times of NTV in a sequence.

Close loop modified SVM with 7, 9 & 13-segment pulse pattern arrangements and delta correction in dwell time is implemented for improved neutral point voltage stabilization. There always exists a small-voltage vector in each switching sequence, whose dwell time is divided into subperiods, one for its P-type and the other for its N-type switching state. For instance, the dwell time ds_{1p} for $\mathbf{u_{S1p}}$ and d_{S1n} for $\mathbf{u_{S1n}}$, which is half/half split normally, can be distributed as

$ds_1 = d_{S1p} + d_{S1n}$

where d_{S1p} and d_{S1n} are given by

$d_{S1p} = ds_1 /2(1+\Delta t)$ and

$d_{S1n} = ds_1 /2(1-\Delta t)$ where $-1 <= \Delta t <= 1$. (1)

The deviation of the neutral point voltage can be further reduced by adjusting the incremental time interval Δt in (1) according to the detected DC capacitor voltages v_{C1} and v_{C2}. The input to the voltage balancing scheme is

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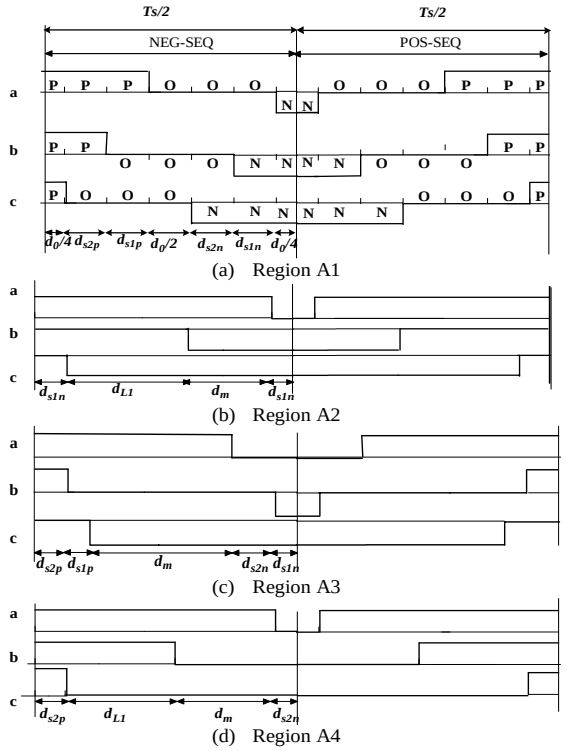

Figure 5. Pulse pattern arrangement of SVM-2 in sector A

the difference in capacitor voltages Δv_C where, $\Delta v_C = v_{C2} - v_{C1}$. If Δv_C is greater than the maximum allowed DC voltage deviation ΔV_m for some reasons, we can increase dwell time d_{S1p} and decrease d_{S1n} by Δt ($\Delta t>0$) simultaneously for the inverter in a inverting mode. A reverse action ($\Delta t<0$) should be taken when the inverter is in a converting mode. The relationship between the capacitors voltage difference and the incremental time interval Δt is summarized in table II.

V. Results and Discussions

Experimental results are obtained on a laboratory prototype of diode clamped 3-level inverter. The DC-link capacitance value of 2200uF is used and DC-link voltage is kept 100 volt. Inductive load having resistance value of 10 ohm and inductance value of 160mH is used. Control is obtained from dSPACE ds1103 R & D controller board and control desk. Fluke 434 power quality analyzer and agilent 54624A oscilloscope have been used for measurements. DC-link voltages are sensed through AD202JN isolation amplifier.

Table II
Relationship between capacitor voltages and incremental time interval Δt

Neutral-point deviation level	Inverting mode	Converting node
$(v_{C2} - v_{C1}) > \Delta Vm$	$\Delta t > 0$	$\Delta t < 0$
$(v_{C2} - v_{C1}) > \Delta Vm$	$\Delta t < 0$	$\Delta t > 0$
$\lvert v_{C2} - v_{C1} \rvert < \Delta Vm$	$\Delta t = 0$	$\Delta t = 0$

ΔVm - maximum allowed DC voltage deviation ($\Delta V_C > 0$)

Figure 6 shows the output waveform quality of the three-level inverter at MI value of 0.8. Harmonic spectrum revels that higher even order harmonic components increases voltage and current THD due to large unbalance in DC-link voltages. Figure 7 shows plot of phase voltage THD versus MI for SVM-1 and SVM-2. Figure 8 shows plot of phase current THD Vs MI for SVM-1 and SVM-2.

Experimental results of the proposed scheme shows reduced voltage and current THD except at very low MI. At MI value of 0.866, dwell times of small vector reduces. DC-link voltage balancing by splitting of small vector becomes inefficient. Control of proposed scheme is more effective in region 1 and 3, where two small vectors are spitted in pulse pattern arrangement for DC-link balancing control. In region 2 and 4, only one small vector is spitted in pulse pattern arrangement for DC-link balancing control. Figure 9 shows plot of neutral point voltage variation verses DC-link voltage for SVM-1 and SVM-2. The neutral point voltage increases to higher value at higher DC-link voltages for SVM-1, where as in proposed scheme it is restricted well below maximum specified value and its variation is lower. In proposed scheme (SVM-2) neutral point voltage is significantly lower then SVM-1.

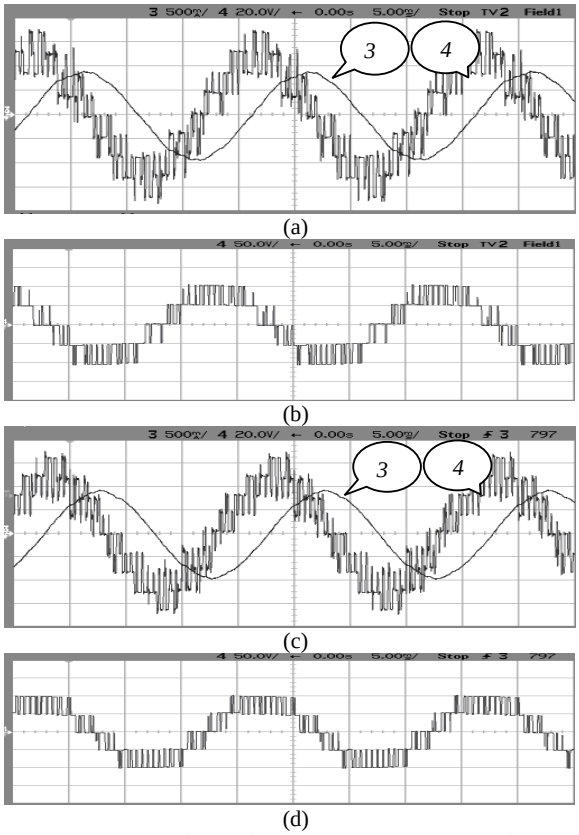

Figure 6. Output waveforms of the three-level inverter at MI of 0.8.
a, c Phase current [trace-3 x-axis: 5 ms/div, y-axis: 500 mA/div] and phase voltage [trace-4 x-axis: 5 ms/div, y-axis: 20 V/div]
b, d Line to line voltage [x-axis: 5 ms/div, y-axis: 50 V/div]
a, b waveforms with SVM-1 and
c, d waveforms with SVM-2

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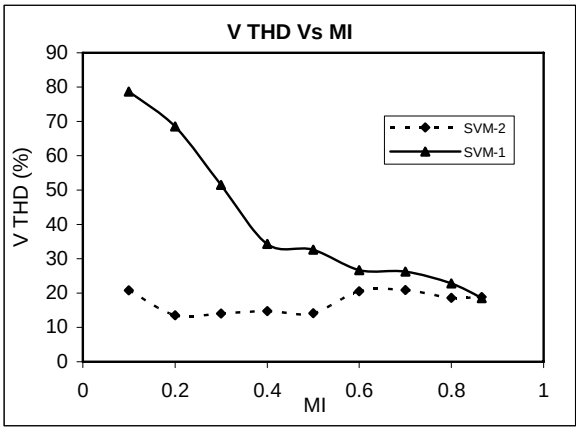

Figure 7. Plot of voltage THD versus MI for SVM-1 and SVM-2.

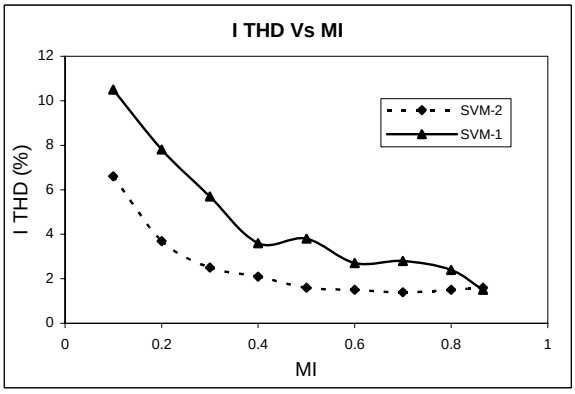

Figure 8. Plot of current THD versus MI for SVM-1 and SVM-2

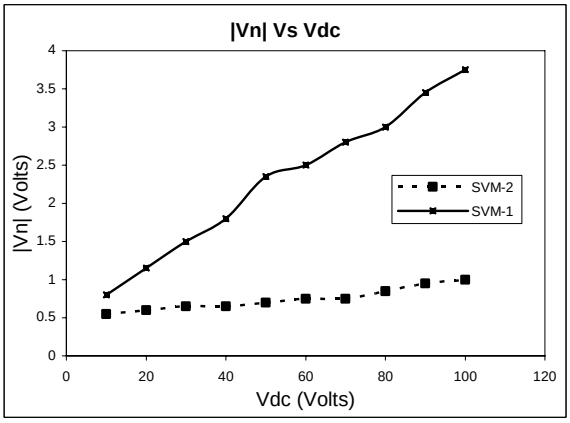

Figure 9. Plot of neutral point voltage variation, |Vn| versus DC-link voltage for SVM-1and SVM-2

VI. Conclusion

The DC-link voltage balancing scheme for three-level diode clamping inverter is investigated in this paper. The detailed analysis investigates the DC-link voltage control behaviour of proposed scheme and popular SVM scheme. The closed loop scheme is used with simple control technique. Redundant space vectors, their sequencing, and splitting of their duty cycle are used for control. Single front-end rectifier can be used with reduced rating DC-link capacitors and reduced rating switches of inverter, which results into saving of cost and volume. The performance of various SVM schemes are evaluated with respect to inverter output voltage THD, current THD and neutral point voltage with respect to various DC-link voltages and modulation index (MI). The proposed scheme gives neutral point voltage reduction along with significant harmonic loss minimization and effective voltage balancing control. Thus, longer life of DC-link capacitors can be achieved.

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